CLAIMS

What is claimed is:

1. An apparatus comprising:

a circular shift register having N data samples to circularly shift a first data sample of the N data samples into a data position at a first clock frequency, the N data samples corresponding to signal received from one of K satellites in a global positioning system (GPS), the N data samples being loaded into the circular shift register at a second clock frequency;

K storage elements to store K code sequences, respectively, each of the K code sequences having N code samples and including a first code sample being written at a code position corresponding to the data position at a third clock frequency, the K storage elements corresponding to the K satellites; and

a code register to store the N code samples loaded from one of the K storage elements at a fourth clock frequency, the fourth clock frequency being K times faster than the first clock frequency.

2. The apparatus of claim 1 further comprising:

a write circuit coupled to the K storage elements to write the K first code samples to the K storage elements, respectively, at the K code positions synchronously with the shifted first data sample.

3. The apparatus of claim 1 further comprising:

a correlator circuit coupled to the circular shift register and the code register to compute a correlation result from the N data samples and the N code samples.

4. The apparatus of claim 1 wherein each of the K storage elements is one of a plurality of flip-flops, a register, a row in a random access memory (RAM).

5. The apparatus of claim 2 wherein the write circuit comprises:

a plurality of decoders coupled to the K storage elements to enable writing the K first code samples to the K code positions synchronously with the shifted first data sample.

6. The apparatus of claim 3 wherein the correlator circuit comprises:

a mapper to map the N data samples and the corresponding N code samples into a plurality of mapper out puts;

an adder to add the plurality of mapper outputs to generate a result sum; and

a subtractor to subtract a bias value from the result sum to generate the correlation result.

7. The apparatus of claim 6 wherein each of the N code samples is a pseudo random noise (PN) code being represented by a one-bit value.

8. The apparatus of claim 7 wherein each of the N data samples is a two-bit with value of one of 01, 10, and 11.

9. The apparatus of claim 8 wherein each of the mapper outputs is two-bit with value of one of 01, 10, and 11.

10. The apparatus of claim 9 wherein the bias value is 44.

11. The apparatus of claim 10 wherein the correlation result is represented by 6-bit including a sign bit.

12. The apparatus of claim 1 wherein N = 22 and K = 12.

13. The apparatus of claim 1 wherein the first clock frequency is two times a coarse/acquisition chip rate of the GPS.

14. The apparatus of claim 1 wherein the second clock frequency is equal to the first clock frequency divided by N.

15. The apparatus of claim 1 wherein the third clock frequency is equal to the first clock frequency.

16. A method comprising:

circularly shifting a first data sample of N data samples in a circular shift register into a data position at a first clock frequency, the N data samples corresponding to signal received from one of K satellites in a global positioning system (GPS), the N data samples being loaded into the circular shift register at a second clock frequency;

storing K code sequences in K storage elements, respectively, each of the K code sequences having N code samples and including a first code sample being written at a code position corresponding to the data position at a third clock frequency, the K storage elements corresponding to the K satellites; and

storing the N code samples loaded from one of the K storage elements in a code register at a fourth clock frequency, the fourth clock frequency being K times faster than the first clock frequency.

17. The method of claim 16 further comprising:

writing the K first code samples to the K storage elements, respectively, at the K code positions synchronously with the shifted first data sample.

18. The method of claim 16 further comprising:

computing a correlation result from the N data samples and the N code samples.

19. The method of claim 16 wherein each of the K storage elements is one of a plurality of flip-flops, a register, a row in a random access memory (RAM).

20. The method of claim 17 wherein writing the K first code samples comprises:

enabling writing the K first code samples to the K code positions synchronously with the shifted first data sample.

21. The method of claim 18 wherein computing the correlation result comprises:

mapping the N data samples and the corresponding N code samples into a plurality of mapper out puts;

adding the plurality of mapper outputs to generate a result sum; and

subtracting a bias value from the result sum to generate the correlation result.

22. The method of claim 21 wherein each of the N code samples is a pseudo random noise (PN) code being represented by a one-bit value.

23. The method of claim 22 wherein each of the N data samples is a two-bit with value of one of 01, 10, and 11.

24. The method of claim 23 wherein each of the mapper outputs is two-bit with value of one of 01, 10, and 11.

25. The method of claim 24 wherein the bias value is 44.

26. The method of claim 25 wherein the correlation result is represented by 6-bit including a sign bit.

27. The method of claim 16 wherein N = 22 and K = 12.

28. The method of claim 16 wherein the first clock frequency is two times a coarse/acquisition chip rate of the GPS.

29. The method of claim 16 wherein the second clock frequency is equal to the first clock frequency divided by N.

30. The method of claim 16 wherein the third clock frequency is equal to the first clock frequency.

31. A receiver comprising:

a mixer to generate mixer output samples from a signal received from one of K satellites in a global positioning system (GPS), the mixer output samples including in-phase and quadrature components;

a pseudo-random noise (PN) code generator to generate PN code sequences; and

a de-spreader circuit coupled to the mixer and the PN code generator to de-spread the mixer output samples, the de-spreader circuit comprising:

a circular shift register having N data samples of the mixer output samples to circularly shift a first data sample of the N data samples into a data position at a first clock frequency, the N data samples corresponding to the signal, the N data samples being loaded into the circular shift register at a second clock frequency,

K storage elements to store K code sequences, respectively, from the PN code generator, each of the K code sequences having N code samples and including a first code sample being written at a code position corresponding to the data position at a third clock frequency, the K storage elements corresponding to the K satellites, and

a code register to store the N code samples loaded from one of the K storage elements at a fourth clock frequency, the fourth clock frequency being K times faster than the first clock frequency.

32. The receiver of claim 31 further comprising:

a write circuit coupled to the K storage elements to write the K first code samples to the K storage elements, respectively, at the K code positions synchronously with the shifted first data sample.

33. The receiver of claim 31 further comprising:

a correlator circuit coupled to the circular shift register and the code register to compute a correlation result from the N data samples and the N code samples.

34. The receiver of claim 31 wherein each of the K storage elements is one of a plurality of flip-flops, a register, a row in a random access memory (RAM).

35. The receiver of claim 32 wherein the write circuit comprises:

a plurality of decoders coupled to the K storage elements to enable writing the K first code samples to the K code positions synchronously with the shifted first data sample.

36. The receiver of claim 33 wherein the correlator circuit comprises:

a mapper to map the N data samples and the corresponding N code samples into a plurality of mapper out puts;

an adder to add the plurality of mapper outputs to generate a result sum; and

a subtractor to subtract a bias value from the result sum to generate the correlation result.

37. The receiver of claim 36 wherein each of the N code samples is a pseudo random noise (PN) code being represented by a one-bit value.

38. The receiver of claim 37 wherein each of the N data samples is a two-bit with value of one of 01, 10, and 11.

39. The receiver of claim 38 wherein each of the mapper outputs is two-bit with value of one of 01, 10, and 11.

40. The receiver of claim 39 wherein the bias value is 44.

41. The receiver of claim 40 wherein the correlation result is represented by 6-bit including a sign bit.

42. The receiver of claim 41 wherein N = 22 and K = 12.

43. The receiver of claim 41 wherein the first clock frequency is two times a coarse/acquisition chip rate of the GPS.

44. The receiver of claim 41 wherein the second clock frequency is equal to the first clock frequency divided by N.

45. The receiver of claim 41 wherein the third clock frequency is equal to the first clock frequency.